(12) UK Patent Application (19) GB (11) 2 211 991 (13) A

(43) Date of A publication 12.07.1989

(21) Application No 8825311.7

(22) Date of filing 28.10.1988

(30) Priority data
(31) 8725497 (32) 30.10.1987 (33) GB

(51) INT CL⁴
H01L 21/76

(52) UK CL (Edition J)
H1K KGCX K11B1 K11B4 K11D K5BX K5B2 K5B5 K5B9 K9D1

(56) Documents cited
None

(58) Field of search
UK CL (Edition J) H1K KGCW KGCX KJAX KKB KLCA KLCB KLCX
INT CL⁴ H01L

(71) Applicant
United Kingdom Atomic Energy Authority

(Incorporated in the United Kingdom)

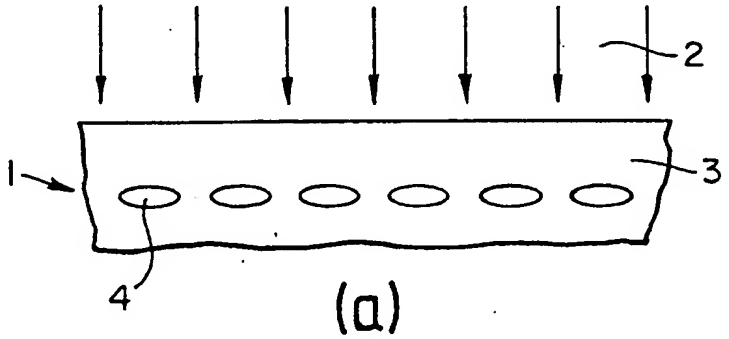
11 Charles II Street, London, SW1Y 4QP, United Kingdom

(72) Inventor
Dr Geoffrey Dearnaley

(74) Agent and/or Address for Service
Paul Austin Wood
United Kingdom Atomic Energy Authority, Patents Branch, 11 Charles II Street, London, SW1Y 4QP, United Kingdom

(54) Electrical isolation of regions within semiconductor bodies

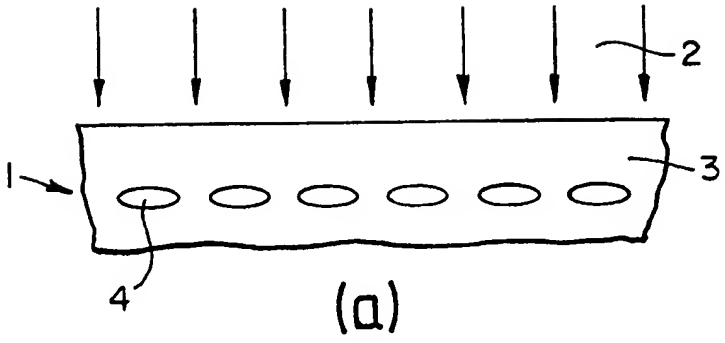
(57) A process for producing a buried dielectric or high-resistivity layer within a body of semiconductor material comprising the operations of implanting ions (2) of hydrogen or an inert gas into the body at an energy and dose such as to form a layer of discrete bubbles and/or voids (4) within the body (3) of semiconductor material and subsequently implanting ions of oxygen or nitrogen into the semiconductor material at an energy and dose such as initially to stabilise the bubbles and/or voids within the semiconductor material and then form a layer of oxide or nitride of the semiconductor material bridging the gaps between the said bubbles and/or voids.



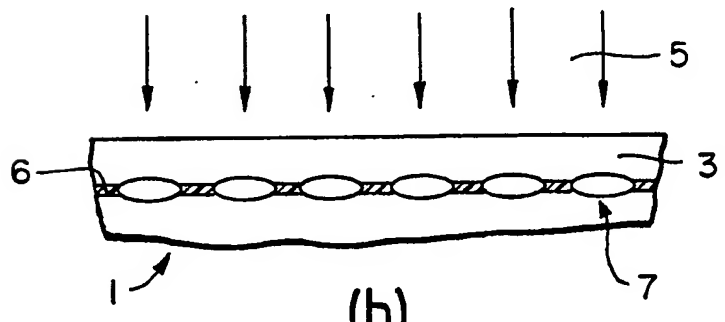
(a)

GB 2 211 991 A

2211991



(a)



(b)

2211991

Electrical Isolation of Regions within Semiconductor Bodies

The present invention relates to the electrical isolation of regions within a body of a semiconductor substance as a step in the production of micro electronic devices.

In order to produce micro electronic devices it is necessary to isolate adjacent elements of the electrical circuit concerned and to provide isolation between active devices and underlying substrate material. It has been shown that this can be done by producing one or more buried layers of high-resistivity or dielectric material within a silicon substrate body by implanting sufficient ions of oxygen or nitrogen to create a continuous layer of silicon oxide or nitride where the ions come to rest in the silicon. However, the ion doses required are very high ($>10^{18}$ ions cm^{-2}) and the process is a difficult one to carry out economically due to the need for high fluxes of ions at energies of 150-200 KeV. It is desirable therefore to find alternative techniques that can be more attractive economically.

It is known that when high doses ($>10^{17}$ ions cm^{-2}) of inert gas ions are implanted into a body of silicon, bubbles of gas are formed within the silicon. If the silicon is then subjected to a post-implantation anneal, there is a tendency both for the bubbles to migrate through the silicon and for the inert gas to diffuse through the silicon and escape from the surface of the silicon so leaving voids in the silicon. It has been found, furthermore, that if oxygen is implanted into the silicon after the inert gas, then, either at the time of bombardment or during a subsequent anneal, it will migrate to the bubbles, associate with them and stop their migration when the silicon is annealed.

According to the present invention there is provided a process for producing a buried dielectric or high-resistivity layer within a body of semiconductor material comprising the operations of implanting ions of hydrogen or an inert gas into the body at an energy and dose such as to form a layer of discrete bubbles and/or voids within the body of semiconductor material and subsequently implanting ions of oxygen or nitrogen into the semiconductor material at an energy and dose such as initially to stabilise the bubbles and/or voids within the semiconductor material and then form a layer of oxide or nitride of the semiconductor material bridging the gaps between the said bubbles and/or voids.

Suitable ion doses and energies for the formation of the bubbles and/or voids are at least 10^{14} ions cm^{-2} and the range 10-100 KeV, respectively. The ion energy required depends on the depth at which it is desired to produce the buried layer of dielectric or high-resistivity material. It is to be noted that the implantation energy required to produce any given penetration for hydrogen is about half that required for helium. Also if hydrogen is implanted to form the bubbles or voids, then the implantation temperature should be kept below about 700°K.

Suitable ion doses for the implantation of the oxygen or nitrogen are at least 10^{14} ions cm^{-2}. The energy required is about twice that for helium ions and five times that required for hydrogen.

Preferably the semiconductor material is silicon.

The invention will now be described by way of example with reference to the accompanying drawing which illustrates the steps involved in producing a buried dielectric layer by a process embodying the invention.

Referring to the drawing, a body 1 of single crystal silicon is subjected to bombardment with a beam 2 of helium ions at an energy of about 75 KeV until a dose of about 10^{15} ions cm^{-2} is implanted. The temperature of the body 1 of silicon is maintained at about 600°K so that recrystallisation of the surface region 3 of the body 1 of silicon occurs continuously as the implanted helium ions pass through it. As a result of this bombardment an array of buried helium-filled bubbles 4 is formed as shown at (a) in the accompanying drawing.

The body 1 of silicon is then subjected to further bombardment with a beam 5 of ions of oxygen having an energy of 200 KeV until a dose of about 10^{15} ions cm^{-2} has been implanted. This time the temperature of the body 1 of silicon is maintained at between 800 and 900°K so as to facilitate the migration of the oxygen through the crystal lattice to the surfaces of the array of bubbles and/or voids 4. (Voids are now present because some of the helium will have diffused out of the bubbles as a result of the heating of the body 1 of silicon). Also, a layer 6 of silicon oxide is formed which bridges the gaps between the bubbles and/or voids 4, thus providing a continuous buried dielectric layer 7, as shown at (b) in the accompanying drawing.

Finally, the body 1 of silicon is annealed in an inert environment such as dry nitrogen in order to stablilise the structure and to remove any residual strain and/or disorder which may be present in the region of the body 1 of silicon above the buried dielectric layer 7.

If desired, the helium ions may be replaced by hydrogen ions and the oxygen ions by nitrogen ions. If the helium is replaced by hydrogen, then although the ion dose remains about the same, the energy required for a given depth of penetration is reduced by a factor of 2. The

temperature of the body 1 of silicon needs to be reduced to about 500°K. The implantation energy and dose of the oxygen or nitrogen remains the same as before.

It should be noted that there is an upper limit to the ion dose of the hydrogen or helium arising from the need to prevent the bubbles and/or voids from being so densely packed that they may coalesce to form a continuous defect which will allow the upper region of silicon to become detached. This ion dose varies with temperature but in general is above 10^{18} ions cm^{-2}.

Also, if required the ion implantations can be carried out through masks which define specific areas of the body of silicon which require to be provided with buried isolation.

As this practice is standard in the art of micro electronic device production it is not thought necessary to describe such a variation of the process according to the invention, specifically.

The invention is not restricted to the details of the foregoing example. For instance, the process might also be applied to other semiconducting materials, such as germanium, gallium arsenide, or layered structures of more than one semiconducting material, for the purpose of providing buried isolation.

Claims

1 A process for producing a buried dielectric or high-resistivity layer within a body of semiconductor material comprising the operations of implanting ions of hydrogen or an inert gas into the body at an energy and dose such as to form a layer of discrete bubbles and/or voids within the body of semiconductor material and subsequently implanting ions of oxygen or nitrogen into the semiconductor material at an energy and dose such as initially to stabilise the bubbles and/or voids within the semiconductor material and then form a layer of oxide or nitride of the semiconductor material bridging the gaps between the said bubbles and/or voids.

2 A process according to claims wherein the operation of forming a layer of discrete bubbles or voids within the body of semiconductor material comprises implanting the ions of hydrogen or inert gas to an ion dose within the range 10^{14}-10^{18} ions cm^{-2} and with an energy within the range 10 - 100 keV, the ion energy being selected so as to form the layer of bubbles or voids at a predetermined depth within the body of semiconductor material.

3 A process according to claim 1 or claim 2 wherein the oxygen or nitrogen is implanted to an ion dose within the range 10^{14}-10^{18} ions cm^{-2} and with an energy such that the ions of oxygen or nitrogen come to rest within the body of semiconductor material at the same depth as the layer of discrete bubbles or voids.

4 A process according to any of claims 1 to 3 wherein the semiconductor material is silicon.

5 A process according to claim 4 wherein there is

included the operations of bombarding the body of silicon with ions of helium having an energy of approximately 75 KeV until an ion dose of approximately 10^{15} ions cm^{-2} has been implanted the body of silicon being maintained at a temperature such that recrystallisation of the surface region of the silicon through which the ions pass occurs, bombarding the silicon body with ions of oxygen or nitrogen having an energy of approximately 200 KeV until an ion dose of approximately 10^{15} ions cm^{-2} has been implanted the body of silicon being maintained at a temperature such as to facilitate the migration of the oxygen or nitrogen through the crystal lattice to the surfaces of the discrete bubbles or voids and the formation of a layer of silicon oxide or nitride bridging the gaps between the discrete bubbles or voids thus providing a continuous buried dielectric layer within the silicon body, and subjecting the body of silicon to an annealing operation.

6 A process according to claim wherein there is included the operations of bombarding the body of silicon with ions of hydrogen having an energy of approximately 40 KeV until an ion dose of approximately 10^{15} ions cm^{-2} has been implanted the body of silicon being maintained at a temperature such that recrystallisation of the surface region of the silicon through which the ions pass occurs, bombarding the silicon body with ions of oxygen or nitrogen having an energy of approximately 200 KeV until an ion dose of approximately 10^{15} ions cm^{-2} has been implanted the body of silicon being maintained at a temperature such as to facilitate the migration of the oxygen or nitrogen through the crystal lattice to the surfaces of the discrete bubbles or voids and the formation of a layer of silicon oxide or nitride bridging the gaps between the discrete bubbles or voids thus providing a continuous buried dielectric layer within the silicon body, and subjecting

the body of silicon to an annealing operation.

7 A process according to claim 5 wherein the body of silicon is maintained at a temperature of approximately 600°K during the bombardment with helium ions and at a temperature within the range 8-900°K during the bombardment with oxygen or nitrogen ions.

8 A process according to claim 6 wherein the body of silicon is maintained at a temperature of approximately 500°K during the bombardment with hydrogen ions and at a temperature within the range 8-900°K during the bombardment with oxygen or nitrogen ions.

9 A process according to any of claims 5 to 8 wherein the annealing process comprises the operation of heating the body of silicon to a temperature of approximately 700°K in an inert atmosphere.

10 A process according to any of claims 1 to 4 wherein the semiconductor material is germanium, or gallium arsenide.

11 A process according to any preceding claim wherein the buried layer is formed within specific regions of the body of semiconductor material only.

12 A process for producing a buried dielectric or high resistivity layer within a body of semiconductor material substantially as hereinbefore described and with reference to the accompanying drawings.

P A Wood
Chartered Patent Agent
Agent for the Applicant

14276 WdH